WHAT IS CLAIMED IS:

1. A semiconductor memory device including:

a semiconducting substrate;

a first diffusion region provided in a substrate surface;

a first insulating film provided in a first area on said substrate neighboring to said first diffusion region;

a first gate electrode provided on said first insulating film;

a second insulating film provided in a second area on said substrate neighboring to said first area; and

a second gate electrode provided on said second insulating film,

wherein said first diffusion region, said first insulating film, said first gate electrode, said second insulating film and said second gate electrode constitute a unit cell;

wherein a second diffusion region is provided in a third area in the substrate surface located in an extension of said second gate electrode; and

wherein, in said unit cell, said first gate electrode intersects said second gate electrode via an insulating film.

2. A semiconductor memory device, including:

a semiconducting substrate;

first and second diffusion regions, provided in separation from each other in a substrate surface;

first and second insulating films, provided in first and second areas on said substrate neighboring to said first and second diffusion regions, respectively;

first and second gate electrodes, provided on said first and second insulating films;

a third insulating film provided in a third area on said substrate neighboring to said first and second areas;

a third gate electrode provided on said third insulating film; and

a fourth insulating film provided on said third gate electrode;

wherein said first and second diffusion regions, said first and second insulating films, said first and second gate electrodes, said third insulating film, said third gate electrode constitute a cell for storing two bits of information;

wherein said first and second gate electrodes are connected in common on said fourth insulating film to constitute a word line electrode;

wherein said third gate electrode constitutes a control gate electrode extending in a direction perpendicular to said word line; and

wherein a third diffusion region is provided in a fourth area in said substrate surface located on an extension of said third gate electrode.

3. A semiconductor memory device comprising:

a semiconducting substrate;

a first diffusion region provided in a substrate surface;

a control gate electrode provided on the substrate with interposition of a first insulating layer, in an area neighboring to said first diffusion region;

a buried diffusion region provided in the substrate surface, at one

or both longitudinal ends of said control gate electrode; and

a first gate electrode provided in an area between said control gate and the first diffusion region with interposition of a second insulating film including a charge trapping film;

wherein said first gate electrode is connected to a word line electrode arranged at right angles to said control gate electrode; and

wherein said first diffusion region, said first gate, said control gate and the buried diffusion region compose a unit cell.

4. A semiconductor memory device comprising:

a semiconducting substrate;

first and second diffusion regions arranged as two rows in a substrate surface in separation from each other;

a control gate electrode arranged in an area on the substrate between said first and second diffusion regions, which form rows, with interposition of a first insulating film;

a buried diffusion region provided in an area in the substrate surface at one or both longitudinal ends of said control gate electrode,

a first gate electrode provided in a first area between said first diffusion region and said control gate with interposition of a second insulating film, including a charge trapping film; and

a second gate electrode provided in a second area between said second diffusion region and said control gate with interposition of a third insulating film, including a charge trapping film, respectively;

wherein said first and second gate electrodes are connected to a word line electrode arranged at right angles to said control gate

electrode; and

wherein said first diffusion region, first gate, control gate and said buried diffusion region constitute a first unit cell and said second diffusion region, second gate, control gate electrode and said buried diffusion region constitute a second unit cell.

5. A semiconductor memory device comprising:

a semiconducting substrate;

first and second diffusion regions, provided in first and second areas in separation from each other in a substrate surface;

a first insulating film provided in a third area between said first and second areas on the substrate;

a first electrically conductive member provided on said first insulating film;

a second insulating film provided on said first electrically conductive member;

third and fourth insulating films provided on both sidewalls of a first gate structure made up by said first insulating film, first electrically conductive member and said second insulating film, with the bottom portions of the third and fourth insulating films abutting on said substrate; said third and fourth insulating films each forming a sidewall of said first gate structure and extending respectively towards said first and second areas; and

a second electrically conductive member provided on said second insulating film;

wherein said second electrically conductive member has first and

second legs protruded towards said substrate into abutment against the sidewall of said third and fourth insulating films;

wherein said first electrically conductive member is arranged at right angles to said second electrically conductive member; and

wherein there is provided a buried diffusion region in the substrate located on at least one longitudinal end of said first electrically conductive member.

6. The semiconductor memory device according to claim 5, wherein said first and second diffusion regions are fabricated by self-alignment using said first electrically conductive member and said first and second legs as masks.

7. The semiconductor memory device according to claim 5, wherein said third and fourth insulating films are each a laminated dielectric film comprising: a silicon oxide film;

a silicon nitride film formed on and overlaying said silicon oxide film; and

a silicon oxide film formed on and overlaying said silicon nitride film.

8. The semiconductor memory device according to claim 5, wherein said second insulating film is a laminated dielectric film comprising:

a silicon oxide film;

a silicon nitride film formed on and overlaying said silicon oxide film; and

a silicon oxide film formed on and overlaying said silicon nitride film.

9. The semiconductor memory device according to claim 5, wherein said first leg of said second electrically conductive member is provided on said third insulating film, in an area between the sidewall of said third insulating film and the first diffusion region;

said second leg of said second electrically conductive member is provided on said fourth insulating film, in an area between the sidewall of said fourth insulating film and the second diffusion region;

wherein fifth and sixth insulating films are provided on said third and fourth insulating films on said first and second diffusion regions, respectively; and

wherein said second electrically conductive member extending on said second insulating film and said fifth and sixth insulating films, constitutes a word line electrode.

10. The semiconductor memory device according to claim 5, wherein said first and second legs of said second electrically conductive member are provided extending from the sidewalls of said third and fourth insulating films to overlie said first and second diffusion regions, respectively.

11. A semiconductor memory device comprising:

a semiconducting substrate;

a plurality of rows of diffusion regions extending in a memory cell area in a substrate surface parallel to one another along one direction in separation from one another, said plural rows of diffusion regions being respectively connected to associated bit lines;

a buried diffusion region extending in said substrate surface in a

direction perpendicular to said one direction at a location spaced apart from both longitudinal ends of said plural rows of diffusion regions;

a plurality of word line electrodes arranged on said substrate with interposition of a first insulating film including a charge trapping film, said word line electrodes extending parallel to one another in a direction perpendicular to said one direction; and

a plurality of control gate electrodes arranged on said substrate in adjacency to an associated one of said diffusion regions, with interposition of a second insulating film, said control gate electrodes each extending along said one direction,

wherein at least one of said control gate electrodes crosses over said buried diffusion region with interposition of said second insulating film.

12. The semiconductor memory device according to claim 11, further comprising:

a plurality of selection transistors on a first side and a second side opposite to said first side of said memory cell area;

the selection transistors of said first side at least including:

a first selection transistor having a first signal terminal, a second signal terminal and a control terminal connected to a first global bit line, a first bit line and to a first selection signal, respectively; and

a second selection transistor having a first signal terminal, a second signal terminal and a control terminal connected to said first global bit line, a second bit line and to a second selection terminal, respectively;

said first and second bit lines being each connected via contact to one end of an associated one of two of said diffusion regions;

the selection transistors of said second side at least including

a third selection transistor having a first signal terminal, a first signal terminal and a control terminal connected to a second global bit line, a third bit line and to a third selection signal, respectively;

a fourth selection transistor having a first signal terminal, a second signal terminal and a control terminal connected to said second global bit line, a fourth bit line and to a fourth selection signal, respectively;

the columns of said diffusion regions, associated with the bit lines connected to said selection transistors of said first side, being arranged alternately with the columns of said diffusion regions associated with the bit lines connected to said selection transistors of said second side.

13. The semiconductor memory device according to claim 12, wherein

a base portion of a first control gate electrode is arranged for extending along the longitudinal direction of said first buried diffusion region, on the substrate between an area where the selection transistors of said first side are arranged and said first buried diffusion region, with interposition of an insulating film;

wherein a first group of said control gate electrodes are arranged on said substrate from the base portion of said first control gate electrode towards said second side, with interposition of an insulating film;

wherein a base portion of a second control gate electrode is arranged for extending along the longitudinal direction of said second buried diffusion region, in a substrate region between an area where the selection transistors of said second side are arranged and said second buried diffusion region, with interposition of an insulating film;

wherein a second group of said control gate electrodes are arranged from the base portion of said second control gate towards said first side, with interposition of an insulating film;

wherein the first group of said control gate electrodes extending at least to said second buried diffusion region;

wherein the second group of said control gate electrodes extending at least to said first buried diffusion region; and

wherein said first group of said control gate electrodes and the second group of said control gate electrodes being arranged alternately in said memory cell area with interposition said diffusion region.

14. The semiconductor memory device according to claim 11, wherein a plurality of memory cells are divided in a plurality of sets, with a plurality of said word line electrodes as a unit; and wherein

said buried diffusion region is provided in an area defined between neighboring sets.

15. The semiconductor memory device according to claim 11, wherein,

when a first positive voltage is applied to a word line electrode selected;

a second voltage equal to a threshold voltage (Vt) or higher by a preset voltage than said threshold voltage is applied to a control gate

electrode of a selected cell;

a ground potential is applied to said buried diffusion region; and

a third positive voltage is applied to a bit line connecting to a diffusion region closer to a storage node as a write target in said cell,

said buried diffusion region operates as an electron supply source to effect programming by source side injection to said storage node.

16. The semiconductor memory device according to claim 11, wherein,

when a ground potential or a negative voltage is applied to said word line electrode;

a fifth positive voltage is applied to a bit line connecting to said diffusion region;

a sixth positive voltage is applied to said control gate electrode; and

a fourth voltage is applied to said buried diffusion region,

cell erasure is effected with a hole barrier being formed in a channel region directly below said control gate electrode.

17. The semiconductor memory device according to claim 16, wherein,

when said fifth positive voltage is applied to all bit lines of said memory cell area;

the totality of said word line electrodes in said memory cell area are set to a ground potential or to a negative voltage; and

said sixth positive voltage is applied to the totality of said control gate electrodes of said memory cell area,

said cells of said memory cell area are erased collectively.

18. The semiconductor memory device according to claim 11, wherein,

when a seventh positive voltage is applied to said buried diffusion region;

an eighth positive voltage is applied to said control gate of a cell to be read;

a ground potential is applied to a bit line connected to the diffusion region closer to a storage node to be read in said cell; and

a ninth positive voltage is applied to the selected word line electrode,

cell data is read with the buried diffusion region as the drain side.

19. The semiconductor memory device according to claim 22, wherein,

when a ground potential is applied to said buried diffusion region;

an eighth voltage is applied to said control gate of a cell to be read;

a seventh positive voltage is applied to the bit line connecting to the diffusion region closer to a storage node to be read in said cell; and

a ninth positive voltage is applied to the selected word line electrode,

a cell data is read with said buried diffusion region as the source side.

20. The semiconductor memory device according to claim 15, wherein the control gate electrode of a cell adjacent to the selected cell is set to a ground potential.

21. A method for manufacturing a semiconductor memory device

comprising the steps of:

depositing on a semiconductor substrate a first insulating film and then depositing a first electrically conductive film on said first insulating film;

depositing a second insulating film on said first electrically conductive film;

patterning a laminated film composed of said first insulating film, first electrically conductive film and the second insulating film to form a control gate;

depositing a third insulating film on the entire surface of said substrate;

depositing a second electrically conductive film on the entire surface of said substrate and subsequently processing said second electrically conductive film in the form of a sidewall on a sidewall section of said control gate which is covered by said third insulating film;

performing ion injection with the control gate and the sidewall of said second electrically conductive film as a mask to form a diffusion region in the substrate surface by self-alignment;

forming a fourth insulating film on the entire substrate surface and subsequently exposing an upper portion of said sidewall of said second electrically conductive film by polishing or etchback; and

depositing a third electrically conductive film on the entire substrate surface and subsequently removing said third electrically conductive film and the sidewall of said second electrically conductive

film to form a word line.

22. The method according to claim 21, wherein said third insulating film is made up by a silicon oxide film, a silicon nitride film and a silicon oxide film.

23. The method according to claim 21, further comprising the steps of

pre-forming a buried diffusion region in said semiconductor substrate; wherein said control gate is extended at least to said buried diffusion region and patterned.

24. A method for controlling a semiconductor memory device comprising:

first and second diffusion layers arranged in two rows in a substrate surface in separation from each other;

a control gate electrode arranged in an area on the substrate between said first and second layers, forming the rows, with interposition of a first insulating layer;

a buried diffusion region provided in an area in the substrate surface at one or both longitudinal ends of said control gate electrode;

a first gate electrode provided in a first area between said first diffusion region and the control gate, with interposition of second insulating film, including a charge trapping film; and

a second gate electrodes provided in a second area between said second diffusion region and the control gate, with interposition of third insulating films, including a charge trapping film;

wherein said first and second gate electrodes are connected to a word line electrode arranged at right angles to said control gate

electrode; and

wherein said first diffusion region, said first gate, said control gate and the buried diffusion region compose a first unit cell, and

said second diffusion region, said second gate, said control gate and the buried diffusion region compose a second unit cell;

said method comprising the steps of:

setting the selected word line electrode to a first positive voltage;

applying a second voltage equal to a threshold voltage (Vt) or higher by a preset voltage than said threshold voltage (Vt) to the control gate electrode of a selected cell;

applying a ground potential to said buried diffusion region; and

applying a third positive voltage to a bit line connecting to a diffusion region closer to a storage node as a write target in said cell, thereby making said buried diffusion region operate as an electron supply source to effect write operation by source side injection to the storage node.

25. The method according to claim 24, further comprising the steps of:

applying a fourth voltage to said buried diffusion region;

setting a ground electrode or a negative voltage to said word line electrode;

applying a fifth positive voltage to a bit line connected to said diffusion region; and

applying a sixth positive voltage to said control gate electrode, thereby effecting cell erasure with a hole barrier being formed in a channel directly below said control gate electrode.

26. The method according to claim 25, further comprising the steps of:

setting a ground voltage or a negative voltage to the totality of the bit lines of said memory cell area;

applying said fifth positive voltage to the totality of bit lines of said memory cell area; and

applying said sixth positive voltage to the totality of the control gate electrodes of said memory cell area,

thereby effecting collective erasure of the cells in said memory cell area.

27. The method according to claim 24, further comprising the steps of:

applying a seventh positive voltage to said buried diffusion region;

applying an eighth positive voltage to said control gate electrode of the cell to be read;

applying a ground voltage to a bit line connecting to the diffusion region closer to a storage node to be read in said cell; and

applying a ninth positive voltage to the selected word line electrode;

thereby effecting read operation with said buried diffusion region as a drain side.

28. The method according to claim 24, further comprising the steps of

applying a ground voltage to said buried diffusion region;

applying an eighth positive voltage to said control gate electrode of the cell being read;

applying a seventh positive voltage to a bit line connecting to the

diffusion region closer to a storage node to be read in said cell; and

applying a ninth positive voltage to the selected word line electrode;

thereby effecting read operation with said buried diffusion region as a source side.

29. The method according to 24, wherein the control gate electrode of the cell neighboring to the selected cell is a at a ground potential.

30. The semiconductor memory device according to 18, wherein

the control gate electrode of the cell neighboring to the selected cell is a at a ground potential.

31. The semiconductor memory device according to claim 19, wherein

the control gate electrode of a cell adjacent to the selected cell is set to a ground potential.

32. A semiconductor memory device comprising:

a semiconducting substrate;

first and second diffusion regions in said surface;

a gate structure including an insulating film provided on a substrate surface between first and second diffusion regions and an electrically conductive member formed on and overlaying said insulating film; and

a third diffusion region in said substrate, spaced apart from said first and second diffusion regions,

wherein a channel, formed in a substrate surface under the gate of the memory cell, is extended from one of said first and second diffusion regions along a direction parallel to the axis specified by said first and

second diffusion regions, and is turned nearly midway between said first and second diffusion regions to extend from the turning to said third diffusion region.

33. The semiconductor memory device according to claim 32, wherein said insulating film includes a charge trapping film.